

Microelectronics

Characterization of Silicon Semiconductor Electronics Using SIMS Backside Depth Profile Analysis

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Vision: As silicon semiconductors continues to shrink, greater demands are placed upon the metrology techniques used to characterize these materials. If downscaling proceeds according to the schedule outlined by the International Technology Roadmap for Semiconductors, many metrology methods in current use will not have sufficient resolution to characterize future generation semiconductors. We envision that backside sample preparation combined with novel instrumental techniques such as C_{60}^{+} cluster ion bombardment will extend the utility of SIMS measurements to the characterization of future generation silicon semiconductors.

Purpose: The purpose of this work is to improve SIMS depth resolution of semiconductors. We accomplish this through the combined use of backside sample preparation, secondary ion image depth profiling and image analysis techniques.

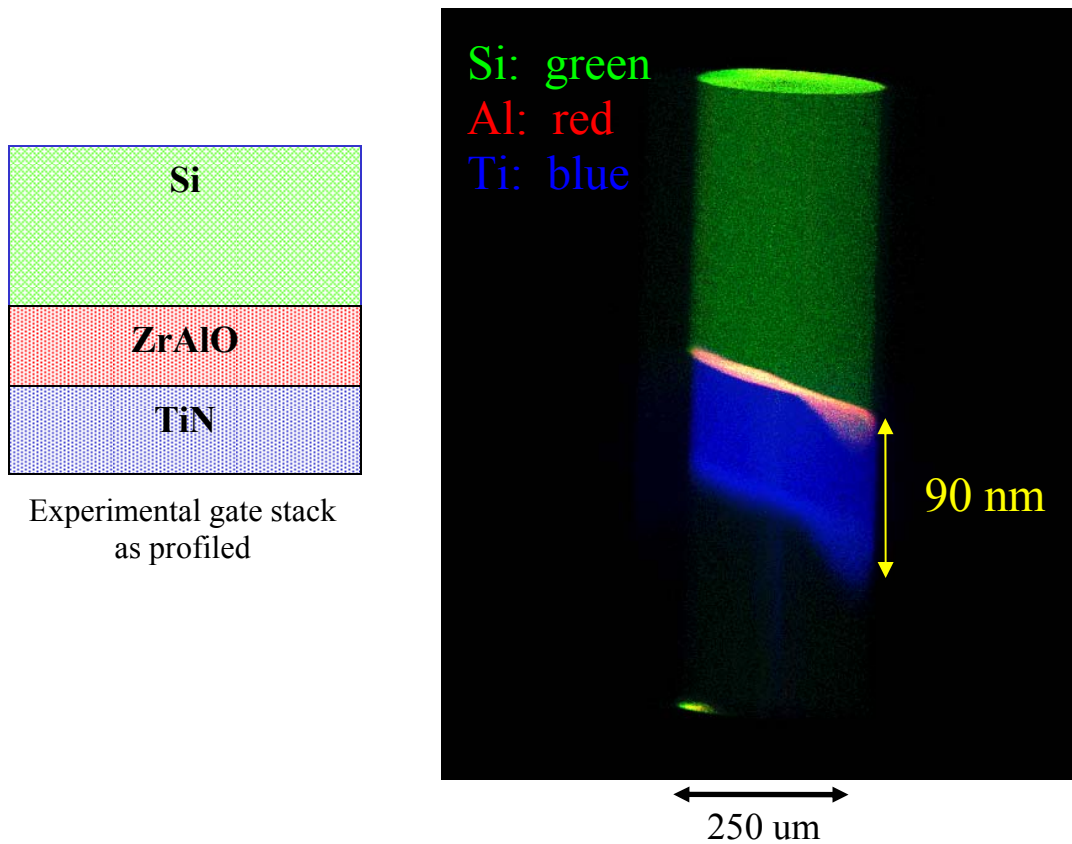
Context: The analytical microscopy group is working together with the Office of Microelectronic Programs at NIST to develop metrology techniques for the characterization of future generation semiconductors. SIMS is a useful characterization tool because the technique has high analytical sensitivity and good depth resolution. State of the art SIMS instruments are capable of reaching sub-micron depth resolution. Such resolution however, is often not achieved when analyzing semiconductors due to limitations imposed by the samples themselves. This is particularly evident in the characterization of shallow dopant profiles and the investigation of diffusion of material through thin gate dielectric films. For both these examples, the analysis area is the ultra-shallow region of the silicon substrate. This region is buried below numerous layers of different materials that were deposited during the manufacturing process. Using SIMS to analyze the area of interest, one must first sputter through these different processing layers. Depth resolution is degraded while sputtering through these layers because of the development of surface topography (especially when sputtering through polycrystalline materials) and the occurrence of knock-on ion beam mixing.

With backside depth profile analysis, high depth resolution is maintained by analyzing the sample from the back (substrate) side rather than the front side. This eliminates the need to sputter through the multiple processing layers on the front side of the wafer.

Major Accomplishments: We have developed a backside sample preparation method that uses mechanical grinding and polishing to remove the silicon substrate prior to SIMS analysis. The method can be applied to a variety of different samples including fully processed, patterned wafers.

We have prepared three-dimensional chemical images that illustrate artifacts produced during the grinding and polishing procedure. This was accomplished using secondary ion image depth profiling techniques to sequentially collect a stack of images during ion sputtering. These images were then combined to produce three-dimensional chemical images. The image below clearly shows the artifact of inclined polishing; the plane of polish is inclined relative to the surface of the sample. If not corrected, this artifact will degrade the resolution of our SIMS analysis.

By applying advanced image analysis techniques to the image stack, we minimized the effect of inclined polishing and improved the depth resolution of our SIMS analysis.



Impact: By improving depth resolution, backside SIMS depth profile analysis should extend the utility of SIMS measurements to the characterization of future generation semiconductor electronic devices.

Future Plans: Future plans include combining backside sample preparation with C_{60}^+ cluster ion SIMS depth profiling to further improve the depth resolution of SIMS measurements.